Attorney Docket No.: 40296-0025

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Cho *et al.*

Confirmation No.: 1058

Application No.: 10/608,103

Art Unit: 2812

Filed: June 30, 2003

Examiner: Jennifer M. Kennedy

For: **METHOD FOR FORMING CAPACITOR OF SEMICONDUCTOR DEVICE**

DECLARATION UNDER 37 C.F.R. §1.132

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

I, Ho Jin Cho, being duly warned, hereby declare and say:

1. I am employed by Hynix Semiconductor Inc. My job title is Senior Member of Technical Staff. I am responsible for capacitor development.

2. I have a Ph.D. degree from Seoul National University. My *curriculum vitae* is attached.

3. I have reviewed the Office Action dated May 18, 2005 in the captioned application. I also have reviewed Kim el al. US 6,580,111 (reference 1), Park et al. 2002/0020869 (reference 2), and Halliyal et al. US 6,645,882 (reference 3).

4. I am informed that in assessing obviousness, the examiner can rely on more than one prior art reference. More specifically, I am informed that the teachings of a collection of references can be combined provided there is some suggestion or motivation to combine the references, and that there is a reasonable expectation of successfully combining the references in order to practice the claimed invention. The obviousness inquiry is made from the standpoint of a person having ordinary skill in the art to which the subject matter pertains at the time the application in question was filed. In summary, claimed inventions are considered obvious only where the prior art provides the person having ordinary skill in the art with a reasonable expectation of successfully practicing the entirety of the claimed subject matter. If the prior art

references lack elements of the claimed invention, contain teachings that render the references not combinable or contain teachings that contrary to the claimed invention, then the claimed invention is not obvious.

5. I believe that it would not have been obvious to a person of ordinary skill in the art to combine reference 3 with references 1 and 2. This is because one skilled in the art would not expect that a dielectric for a gate electrode disclosed in reference 3 would be suitable for use as a dielectric material of a capacitor as described in reference 1. For a gate electrode, the surface characteristics and threshold voltage stability would be considered by the person of ordinary skill in the art when selecting a dielectric. In contrast, leakage current and dielectric constant value are more important factors to be considered in employing the dielectric material for a capacitor.

6. Halliyal et al. (reference 3) discloses a method wherein the dielectric film has a stacked structure of a HFO_2-Al_2O_3 film. However, this reference discloses fabrication of metal oxide semiconductor field effect transistors (MOSFET) (see column 1, lines 11-22 and column 5, lines 31-37). In contrast, references 1 and 2 concern capacitors.

7. Figure 1 attached hereto depicts a plot of gate current density (A/cm^2) against the gate voltage (V) as published in Y. Taur, IEEE (1997 International Electron Devices Meeting IEDM). Figure 2 attached hereto depicts a plot of gate current (A/cm^2) against the thickness (A^o) of a gate oxide and utilizes data obtained from experiments conducted in our own facility. As shown in these figures, the leakage current of a gate oxide ranges from 1 to 100 A/cm^2. In contrast, the leakage current of a dielectric material of a capacitor is usually less than 1×10^{-7} A/cm^2. Therefore, the leakage current of a dielectric material of a capacitor substantially differs from that of the dielectric for a gate electrode by 7 to 9 logs. Accordingly, it would not be obvious to one of ordinary skill in the art to replace the dielectric material of a capacitor with the dielectric material of a gate electrode given the 7 to 9 log difference in leakage current.

8. Given the difference in leakage current, I find no teaching or suggestion in references 1 and 2 to combine them with reference 3 to teach the claimed invention. In fact, I believe the vast difference in leakage current would discourage the person of ordinary skill in the art from combining teachings of gate electrodes with teachings of capacitors.

9. I further declare that I can read English or that I have read a translation of this declaration, that all statements made herein of my own knowledge are true and that all statements

made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent resulting therefrom.

15/9/2005
Date

Dr. Ho Jin Cho, Ph.D.
Senior Member of Technical Staff
Hynix Semiconductor Inc.

Resume

Name in Full: **Ho Jin Cho**
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EDUCATIONS

1. Mar. 1993 ~ Aug. 1997: 「**Ph. D**」 **in Department of Materials Science and Engineering, Seoul National University,** Seoul, Korea. Thesis: Preparation and Dielectric Properties of (Ba,Sr)TiO3 Thin Films by Metal Organic Chemical Vapor Deposition, Advisor: Hyeong Joon Kim (Ph.D., North Carolina State University, 1985).
2. Mar. 1991 ~ Feb. 1993: 「**MS**」 **in Department of Materials Science and Engineering, Seoul National University,** Seoul, Korea. Thesis: Effect of Reaction Products in Monocrystalline β-SiC/Metal Contact on Contact Resistivity, Advisor: Hyeong Joon Kim (Ph.D., North Carolina State University, 1985).
3. Mar. 1987 ~ Feb. 1991: 「**BS**」 **in Department of Materials Science and Engineering, Seoul National University,** Seoul, Korea.

BUSINESS BACKGROUND

1. Sep. 1997 ~ present: Have worked in Hynix Semiconductor Inc.
R&D Division for the Diffusion & Capacitor Technology Development

2. Mar. 2003 ~ present : Senior Member of Technical Staff of Fab Technology Diffusion Team

1) SIS Al2O3, Al2O3/HfO2 Capacitor Process Development for 90nm DRAM
2) MIM HfO2 Capacitor Process Development for 80nm DRAM

3. Jun. 2001 ~ Feb. 2003: Member of Technical Staff of Fab Technology Diffusion Team

   1) MIS TaON Capacitor Process Development for 512M DDR DRAMs
   2) NO Capacitor Process Development for 256M DDR DRAMs

4. Sep. 1997 ~ May. 2001: Member of Technical Staff of Advanced Process Dept. 4
   1) Noble-MIM BST Capacitor Process Development for 0.1 ㎛ Technology
   2) Development of Low Temperature BST MOCVD Process